NASA TECHNICAL MEMORANDUM

NASA TM X-1892

A METHOD FOR SEPARATING A SEMICONDUCTOR WAFER INTO INDIVIDUAL CHIPS

by I. Litant

Electronics Research Center

Cambridge, Mass.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • OCTOBER 1969

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA TM X-1892		

4. Title and Subtitle	5. Report Date
A Method for Separating a Semiconductor Wafer into Individual Chips	October 1969
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
I. Litant	C-85
9. Performing Organization Name and Address	10. Work Unit No.
Electronics Research Center Cambridge, Mass.	125-25-02-14-25
	11. Contract or Grant No.
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Technical Memorandum
National Aeronautics and Space Administration Washington, D.C. 20546	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

A method has been devised to improve the breaking of a semiconductor single-crystal wafer into chips. A scribed wafer placed face-up on a convex surface is contacted rapidly by a rubber diaphragm under air pressure. A stress is thereby applied uniformly in all directions at once causing essentially complete breakage along pre-scribed lines. Dust and debris are minimized.

17. Key Words	18. Distribution Statement
.Semiconductor Single-Crystal Wafer .Scribed Wafer .Rubber Diaphragm .Breakage along Pre-scribed Lines	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No of Pages	22. Price*
Unclassified	Unclassified	14	$3.00

*For sale by the Clearinghouse for Federal Scientific and Technical Information Springfield, Virginia 22151

A METHOD FOR SEPARATING A SEMICONDUCTOR WAFER INTO INDIVIDUAL CHIPS

By I. Litant
Electronics Research Center

SUMMARY

A method is described for rapid separation of the many microcircuits which are present on a single-crystal semiconductor wafer. Present chip separation techniques are an important source of yield loss caused by improper breakage, scratching of the surface, and the production of much debris.

The method comprises placing a rubber diaphragm over a scribed wafer placed face-up on a convex surface and then suddenly applying air pressure over the diaphragm. In this way, a stress is applied uniformly to the wafer to cause breakage along pre-scribed lines, in all directions at once, into predetermined chip sizes.

INTRODUCTION

The processes involved in the manufacture of semiconductor devices, diodes, transistors and integrated circuits are manifold and require that great attention be paid to the minutest details. From the growing of the single crystals of silicon or germanium to the complete packaged device, there are hundreds of processing steps, each of which is vital to the final performance.

When all the dopant diffusions have been made, the dielectric films and metallizations accomplished and the many devices on each wafer have been tested, the wafers must be separated into individual chips so that each may be packaged to operate as a single entity. Each wafer may contain anywhere from a few to hundreds of devices depending on the complexity of the device. The dimensions of the device may vary from 15 x 20 mils to several hundred mils on a side. The wafers themselves, on the other hand, may vary from about 5 mils to 12 mils in thickness and from 1 inch to 2 inches in diameter. The devices are generally spaced from each other on the wafer by a distance of approximately 3 mils to allow for their separation (Figure 1).

Early means of separation of the devices used diamond saws, ultrasonic cutters, or etching. These have given way to diamond scribing and breaking because of the large losses of material entailed in these processes. Despite some drawbacks, diamond scribing is now generally used throughout the industry.

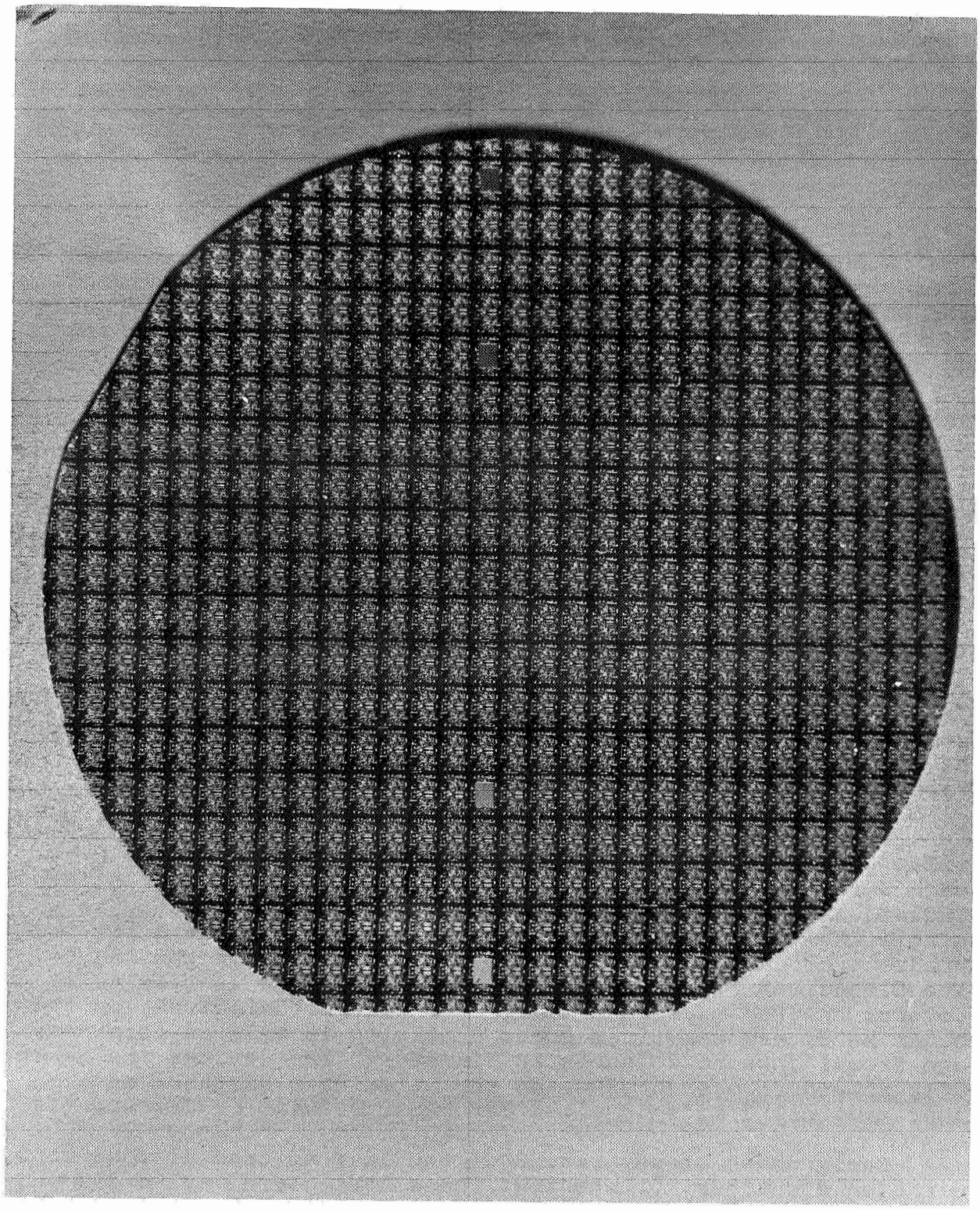


Figure 1.- Scribed wafer

PROCEDURE

Going back one step, scribing and dicing (as the breaking of the wafer is sometimes called) can be no better than the proper lattice orientation in the single-crystal wafers (ref. 1). The usual crystal orientation for the device on a silicon wafer is with its surface in a (111) plane. An orientation flat on the wafer lies in the (110) plane. The (111) planes of a silicon wafer are its natural cleavage planes. If the scribe lines are made in the direction of these planes, then any stressing of the crystal will cause the propagation of the scribe lines into these (111) planes, and clean fracture surfaces result. If the masks are not properly aligned, or if there are large faults in the crystal lattice, secondary cleavage fractures on diagonals may result, with reduced yield.

Proper scribing is also vital to the dicing operation. The selection of the diamond tool and accuracy of the scribing machine are only first steps. Care must be taken to discard the scriber at the first signs of chipping, else conchoidal fractures are created and minute fractures are started that can later propagate and split the chip.

R. L. Beadles (ref. 2) has stated, "Varying somewhat among organizations, the chip separation process has been an important source of yield loss due to breakage and scratching. Since the investment per chip to this stage is small more attention has been given to later processes. Scribing and breaking yields of about 75 percent have been found in pre-mount visual inspections .... cracks, chips, and scratches which are incipient failures may readily pass both this and later tests, only to fail in use. This emphasizes the importance of the scribing and breaking operation in obtaining high reliability integrated circuits."

As integrated circuits become more complex and the wafer more valuable in terms of the increasing number of processing steps invested, the scribing and dicing operations increase in importance.

Various methods are used to separate the scribed silicon wafer into chips. Common to all is the bending of the wafer to stress the scribed lines. The cracks which were introduced during scribing are propagated through the wafer. One method involves laying the wafers on a rubber mat or between plastic films and passing over them with a roller. Another requires placing the scribed wafer in a folded sheet of paper and pulling it down on a curved metal cylinder with scribed side up. Yet another involves mounting the wafer on a steel sheet which is flexed. The difficulty arises in the inherent production of

silicon particles. In most of these procedures, there is sufficient agitation of the breaking and already broken wafer to enable dust particles or an edge of a chip to scratch the surface metallization. These accidents are difficult to see, but nevertheless provide an incipient danger. With the metallization lines being stressed by carrying greater current, even a small reduction in cross section could provide a hot spot.

A new wafer separation method has been devised which uses a portion of a hemisphere on which the scribed wafer is placed, face up. A thin rubber sheet is suspended over the wafer. When air pressure is applied suddenly above this sheet, the stress is transmitted uniformly to the wafer, and it bends to conform to the curvature of the hemisphere, causing the wafer to break along the scribe lines in all directions. By breaking the chips *away* from each other, and all breaking taking place at once, the possibility of surface abrading against surface to produce dust and debris is minimized. A disc is selected with a radius of curvature for optimum performance for the size chip. Following this, there are few operator prerogatives, since the conditions are set and the operation occurs in one step. Yields of close to 100 percent were obtained except where crystal lattice deformations caused diagonal cracks to develop. Wafer thicknesses ranged from 6 to 11 mils.

Figure 2 shows an expanded view of the instrument. The transparent discs at the lower left are spacers for the various hemispheres at lower right. The cover at upper left has in its center the rubber sheet which is pressed down on the wafer by air pressure. In Figure 3 a notched disc is being placed in the well. The notches permit the escape of air compressed by the rubber membrane. In Figure 4 the scribed wafer enclosed by two sheets of 1/4-mil film has been positioned face-up and the cover about to be set in place. Figure 5 shows the quick open-close clamp in position and the device ready to operate. The toggle switch is opened quickly, admitting compressed gas at 120 psi. The pressure is then released, the apparatus opened, and the broken wafer removed as shown in Figure 6.

Figures 7 and 8 show chips which were separated by this process. The triangles were an exercise to demonstrate the versatility of the apparatus.

CONCLUSION

In summary, an apparatus has been developed for the separation of chips in a scribed, single-crystal semiconductor wafer. The advantages are: 1) minimization of formation of dust and debris, 2) a one-operation process that virtually eliminates operator perogatives, and 3) the ability to handle thin or thick wafers in a variety of sizes and shapes.

REFERENCES

1. Beadles, R. L.: Integrated Silicon Device Technology. Technical Documentary Report ASD-TDR-63-316, Vol. XIV, May 1967.

2. Sharif, L. E., Smith, B., and Montgomery, R.: Mechanisms of Scribing and Breaking of Silicon Slices. Proc. of Electrochemical Society Meeting, San Francisco, May 9-13, 1965.

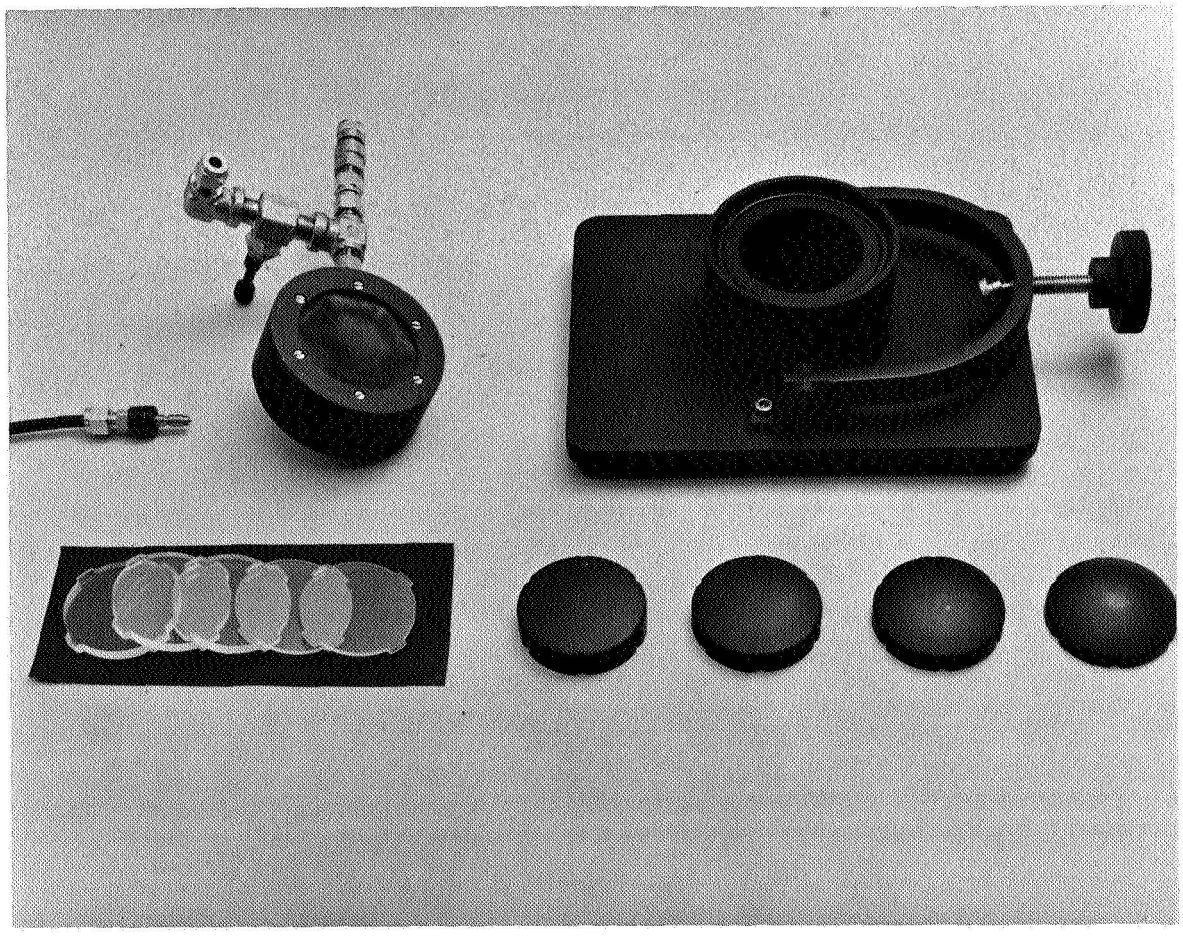


Figure 2.- Expanded view of instrument

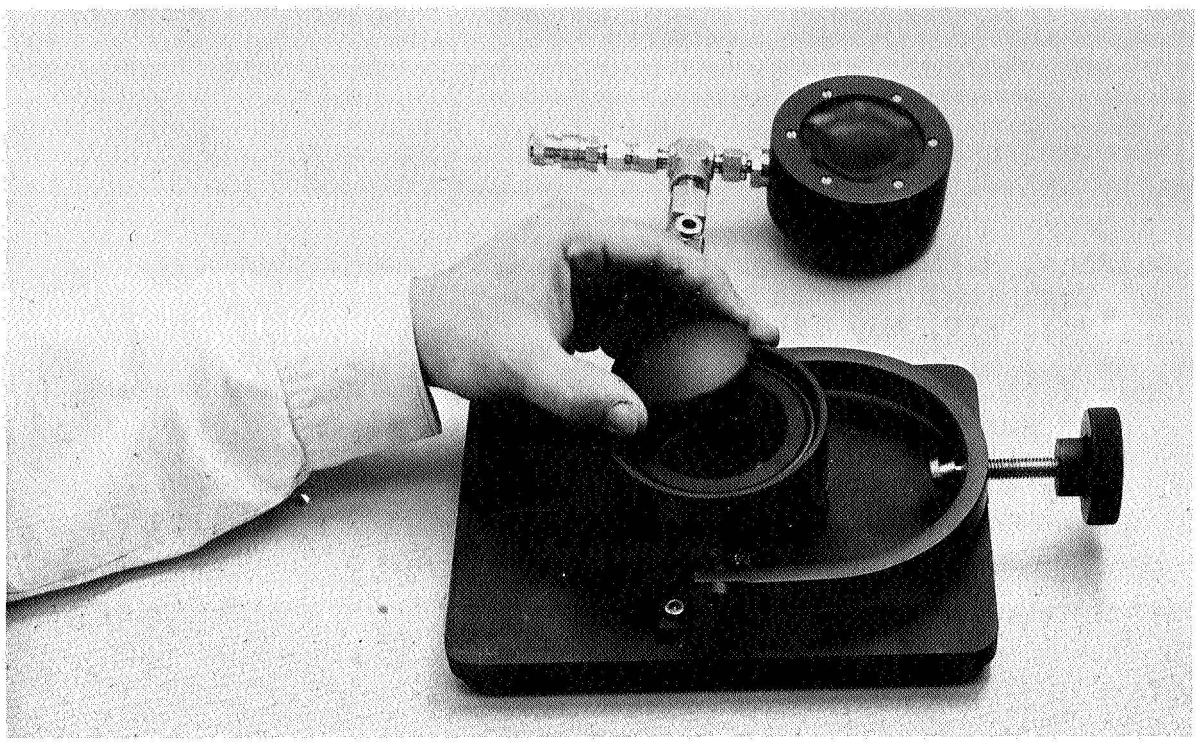


Figure 3.- Scribed wafer placed in position

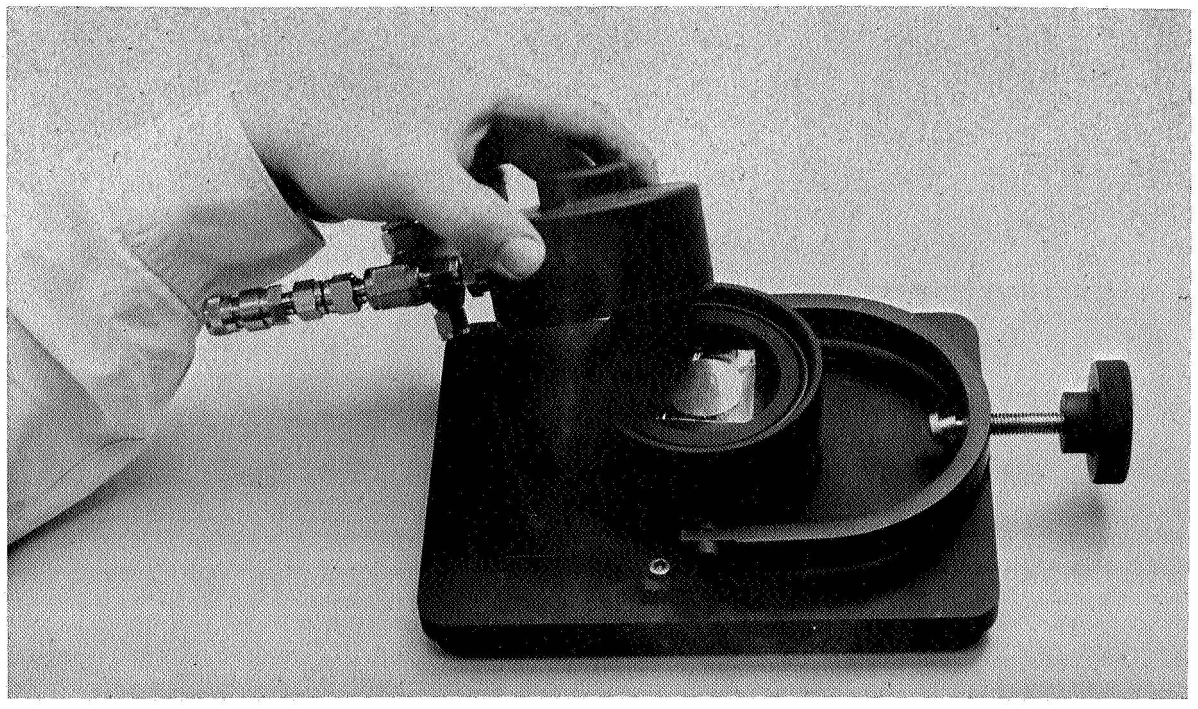


Figure 4.- Notched disc being placed in well

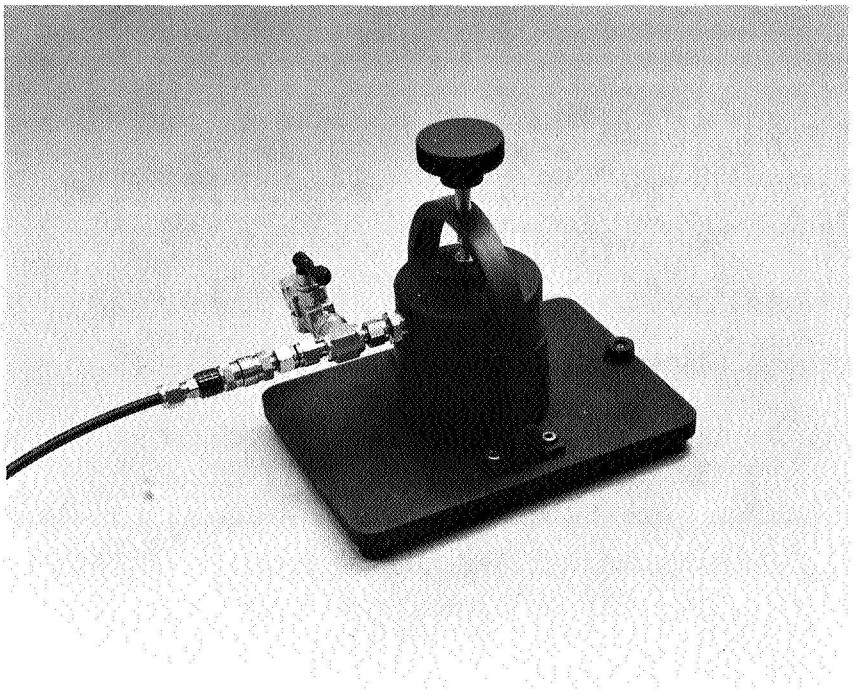


Figure 5.- Quick open-close clamp in position

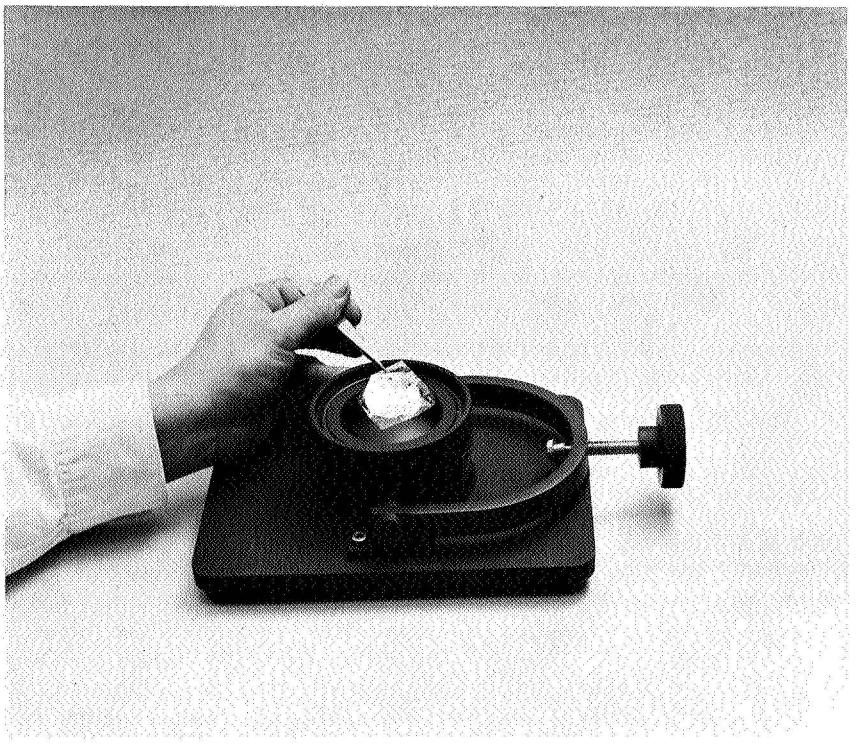


Figure 6.- Broken wafer removed

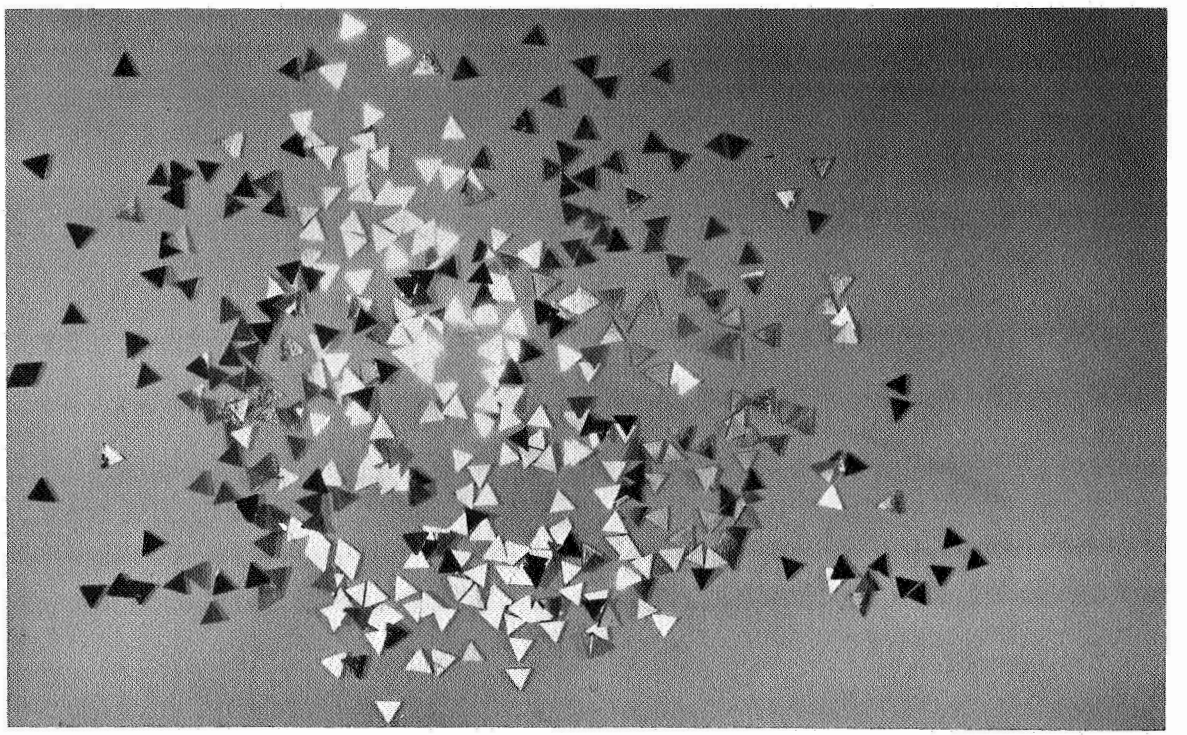


Figure 7. - Separated chips (triangle 60^{o} x 60^{o} x 60^{o} each side measuring .070")

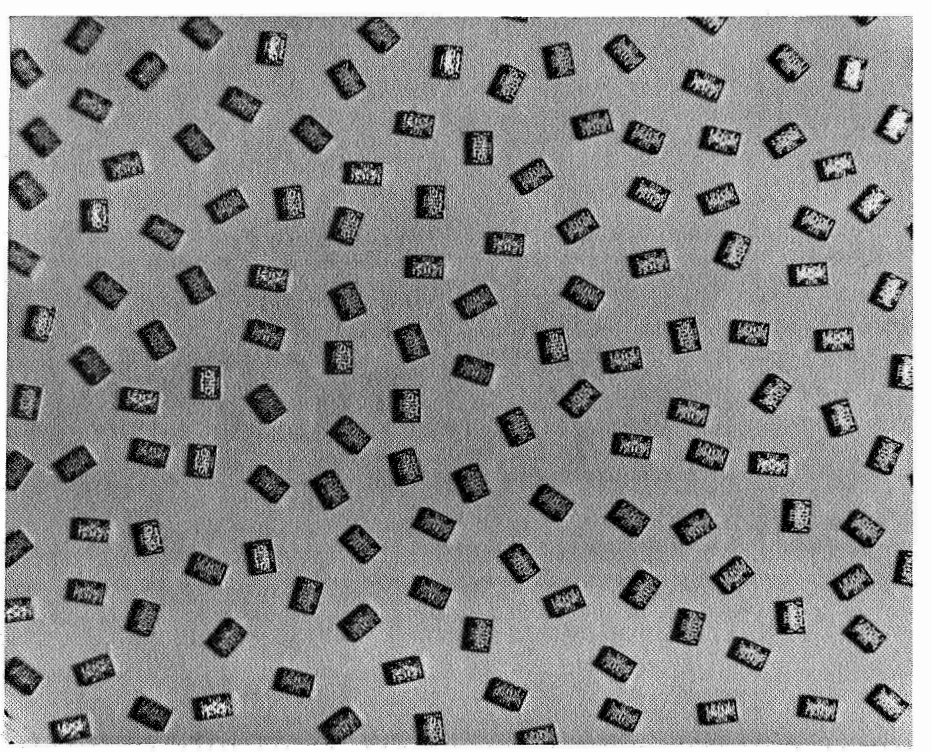


Figure 8. - Separated chips

APPENDIX

ANALYSIS OF SEMICONDUCTOR WAFER DICING PROCESS

S. M. Spitzer
Electronics Research Center

INTRODUCTION

A new technique has been proposed for the dicing of silicon wafers. In this technique, the wafer is placed upon a spherical surface, and gas pressure forces an elastic membrane against the wafer, thus bending it to conform with the spherical surface. Since the wafer will have been scribed, the stresses resulting from bending will cause the wafer to fracture.

It is the intent of this calculation to form a simple model of the wafer during bending, in order to develop a mathematical relationship between the radius of curvature of the spherical surface, and the wafer thickness and chip size. In order to simplify the problem, all chips will be assumed square in order to introduce symmetry. This symmetry permits a one-dimensional analysis, analogous to a beam being deflected over a cylindrical surface.

CALCULATION

The geometry used in this calculation is shown in Figure A-1. The critical points to be examined are where two chips must be bent enough to fracture them (Figure A-1b), yet one chip itself must not be fractured (Figure A-1c).

The maximum tensile stress, σ in the beam is

$$\sigma = MC/I \tag{A-1}$$

where M = bending moment
C = half thickness of beam ($t/2$)
and I = moment of inertia

The maximum bending moment is

$$M = L\left[\frac{I^2}{2}\right] \tag{A-2}$$

where L = loading, weight/length

The moment of inertia for a rectangular beam is

$$I = xt^3/12 \tag{A-3}$$

The maximum deflection, δ, is readily found to be

$$\delta = \frac{L^4}{8\ EI} \tag{A-4}$$

where E = Young's modulus

We note that the deflection, δ, from the horizontal is found to be

$$\delta = r - (r^2-\ell^2)^{1/2} \tag{A-5}$$

where r = spherical radius of curvature.

A Taylor series expansion yields

$$\delta = \frac{\ell^2}{2r}\left[1 + \frac{\ell^2}{4r^2}\right]. \tag{A-6}$$

We are now in a position to relate the physical constants of the model with the radius of curvature and chip size. Equation (4), using equations (1-3), is equated to equation (6). The result is

$$\sigma = \frac{Et}{r}\ (1+\ell^2/4r^2) \tag{A-7}$$

This equation may be conveniently rewritten as

$$r^3 - \frac{Et}{\sigma}r^2 - \frac{Et\ell^2}{4\sigma} = 0 \tag{A-8}$$

Since a cubic equation is somewhat difficult to solve, we will attempt a solution through approximation. Assume $r = r_0 + r' + r'' +\ldots$, and find r_0 using only the first order term of equation (6),

$$r_0 = \frac{Et}{\sigma}\ . \tag{A-9a}$$

Reiterative processes yield

$$r' = \frac{\ell^2}{4r_0} \tag{A-9b}$$

$$r'' = \frac{r_0\ell^2}{4r_0^2 + \ell^2} \tag{A-9c}$$

We wish now to check the validity of this series solution, i.e., show that $r'/r_0 << 1$. Now r_0 is on the order of several inches, while ℓ at most is 0.2 inch. So:

$$r'/r_0 = \frac{\ell^2}{4r_0^2} \simeq 10^{-3}$$

and this expansion is valid.

Looking at the case of two chips to be separated, $\ell = x$ and $t = t'$, the wafer thickness at the scribe line. In this case we must consider the maximum tensile stress strength for silicon (in order to ensure fracture). Thus the pertinent equation, $r = r_0 + r'$, is

$$r' = \frac{Et'}{\sigma_{max}} \qquad \text{(A-10a)}$$

$$r' = \frac{x^2}{4r_0} \qquad \text{(A-10b)}$$

For the case of the single chip, $\ell = x/2$ and t = wafer thickness. In this configuration, we must consider the minimum tensile stress strength (to ensure that the single chip will not fracture). The pertinent equation here, $r = r_0 + r'$, is:

$$r_0 = \frac{Et}{\sigma_{min}} \qquad \text{(A-11a)}$$

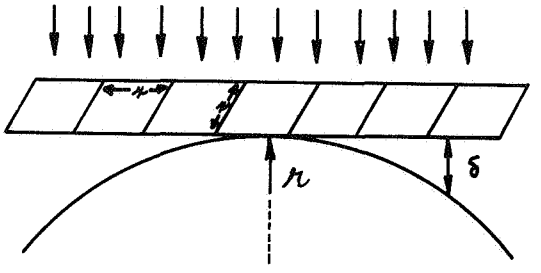
$$r' = \frac{x^2}{16r_0}$$

CONCLUSION

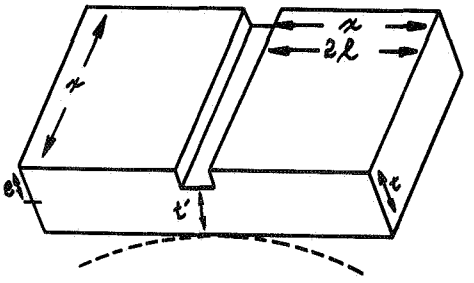
Equations (10a) and (10b) yield an expression for the minimum acceptable radius of curvature, while equations (11a) and (11b) yield an expression for the maximum radius of curvature. Thus the two expressions give a spread of acceptable sphere sizes. It must be noted that the tensile strength of silicon depends upon crystallinity, doping, surface treatment, etc. For this reason there is a wide range between min. and max. Current data are:

$$\sigma_{min} \simeq 2.8 \times 10^4 \text{ psi}$$
$$\sigma_{max} \simeq 5.0 \times 10^4 \text{ psi}$$
$$E \simeq 2.8 \times 10^7 \text{ psi}$$

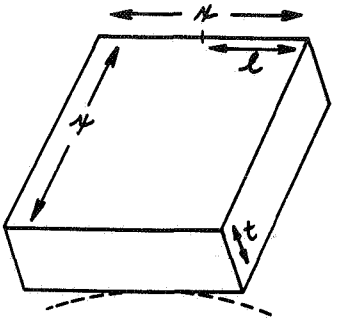
Using these numbers, the graph of Figure A-2 shows the range of radii of curvature as a function of wafer thickness and scribe line depth. Note that for chip size less than 200 mils, the radius of curvature is unaffected because the r' correction term is less than one percent.



a) Scribed silicon beam



b) Case of two chips to be fractured



c) Single chip not to be fractured

Figure A-1.- Calculation geometry.

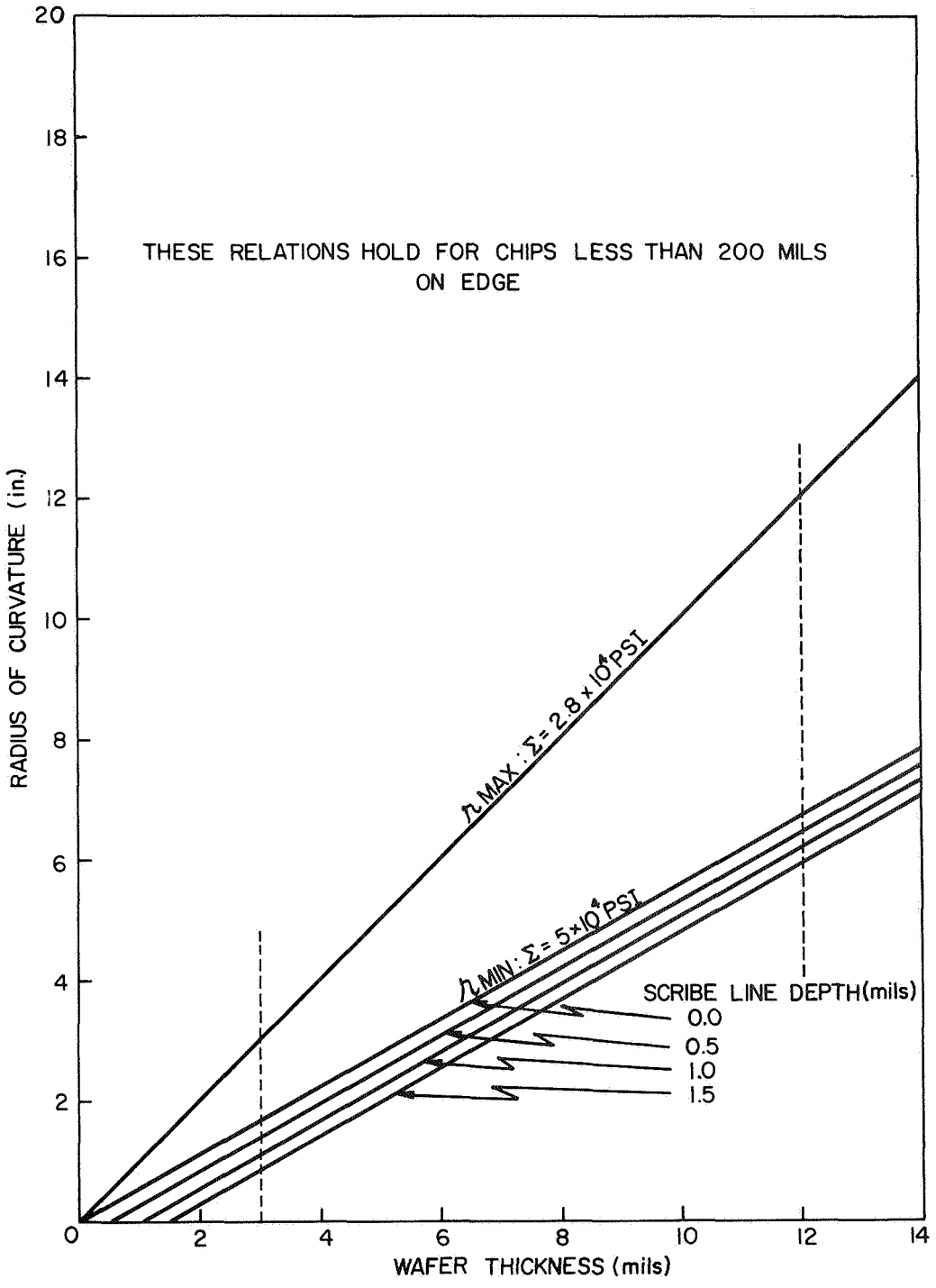


Figure A-2. - Curvature vs. wafer thickness and line depth

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
WASHINGTON, D.C. 20546

OFFICIAL BUSINESS

FIRST CLASS MAIL

POSTAGE AND FEES PAID
NATIONAL AERONAUTICS AND
SPACE ADMINISTRATION

POSTMASTER: If Undeliverable (Section 158
Postal Manual) Do Not Return

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Scientific and technical information generated under a NASA contract or grant and considered an important contribution to existing knowledge.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

TECHNOLOGY UTILIZATION PUBLICATIONS: Information on technology used by NASA that may be of particular interest in commercial and other non-aerospace applications. Publications include Tech Briefs, Technology Utilization Reports and Notes, and Technology Surveys.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546